EXHIBIT E

PWR-SMP240

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 40 W from rectified 220/240 VAC input, 20 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller
- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-In Self-protection Circuits
- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

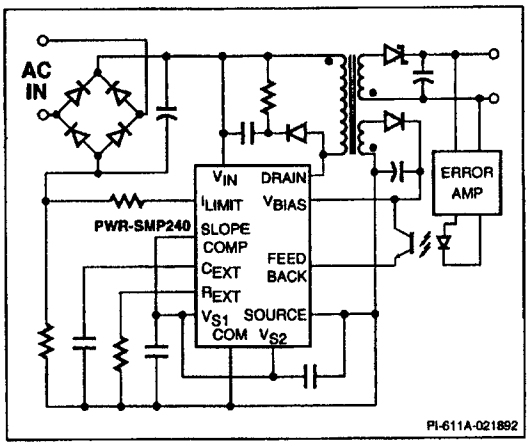

Figure 1. Typical Application

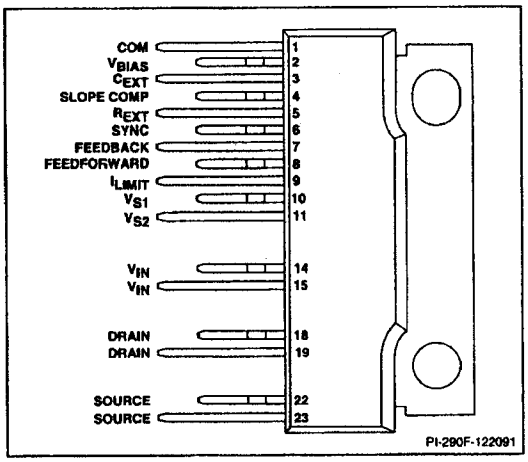

Figure 2. Pin Configuration

Description

The PWR-SMP240, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP240 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP240 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP240WTC	23-pin PWR SIP	0 to 70°C

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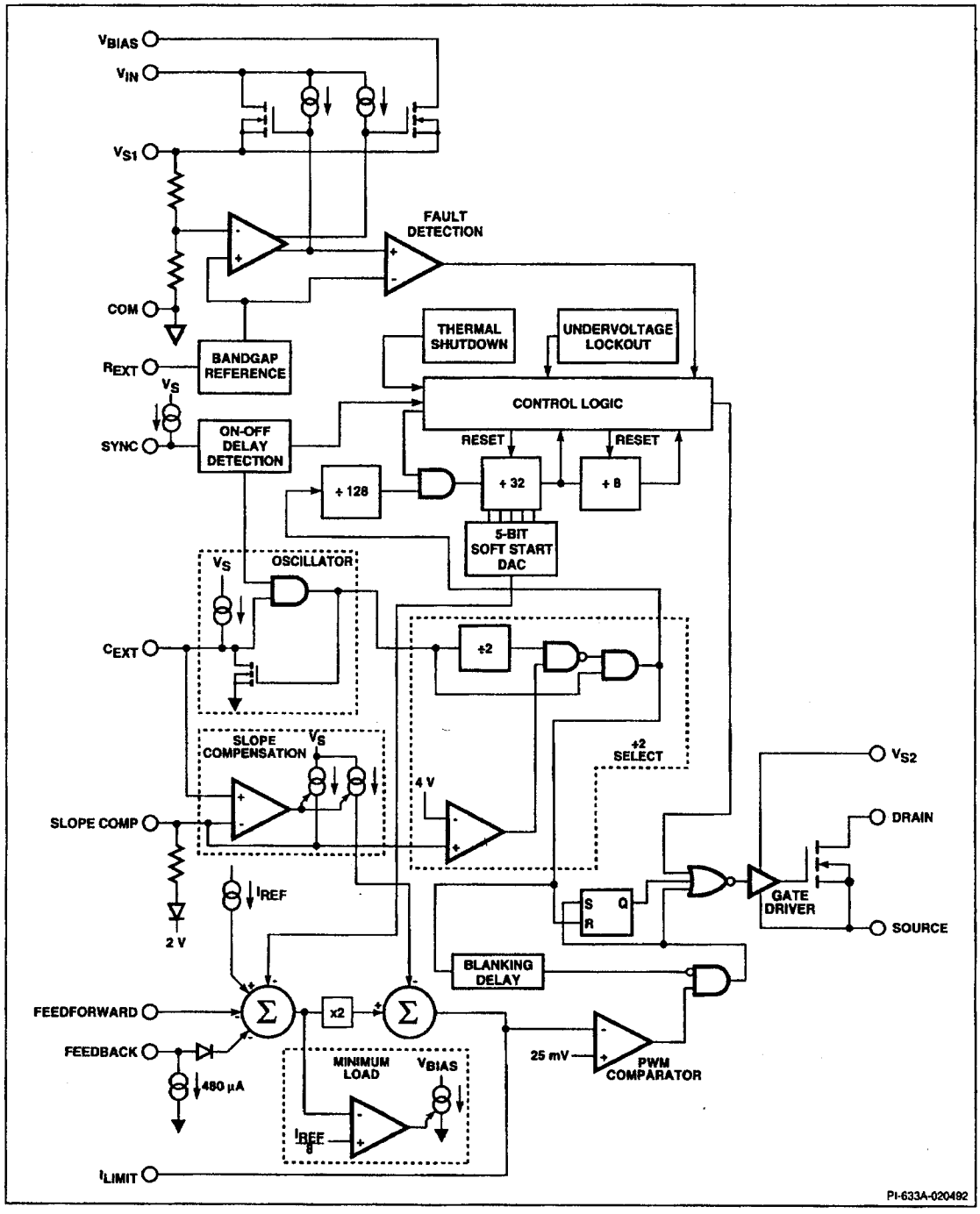

Figure 3. Functional Block Diagram of the PWR-SMP240.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
V_{BIAS} is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance between C_{EXT} and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connction through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between R_{EXT} and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
I_{LIMIT} is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
V_{S1} is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via V_{S2}. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open **DRAIN** of the output MOSFET.

Pin 22, 23:
The **SOURCE** is the high-current return for the output MOSFET.

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PWR-SMP240 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP240 Functional Description (cont.)

Oscillator
The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care should be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator
The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start
The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the Ilimit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit
The undervoltage protection circuit insures that the output transistor is off until the V_{SI} is regulated.

Overtemperature Protection Circuit
The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

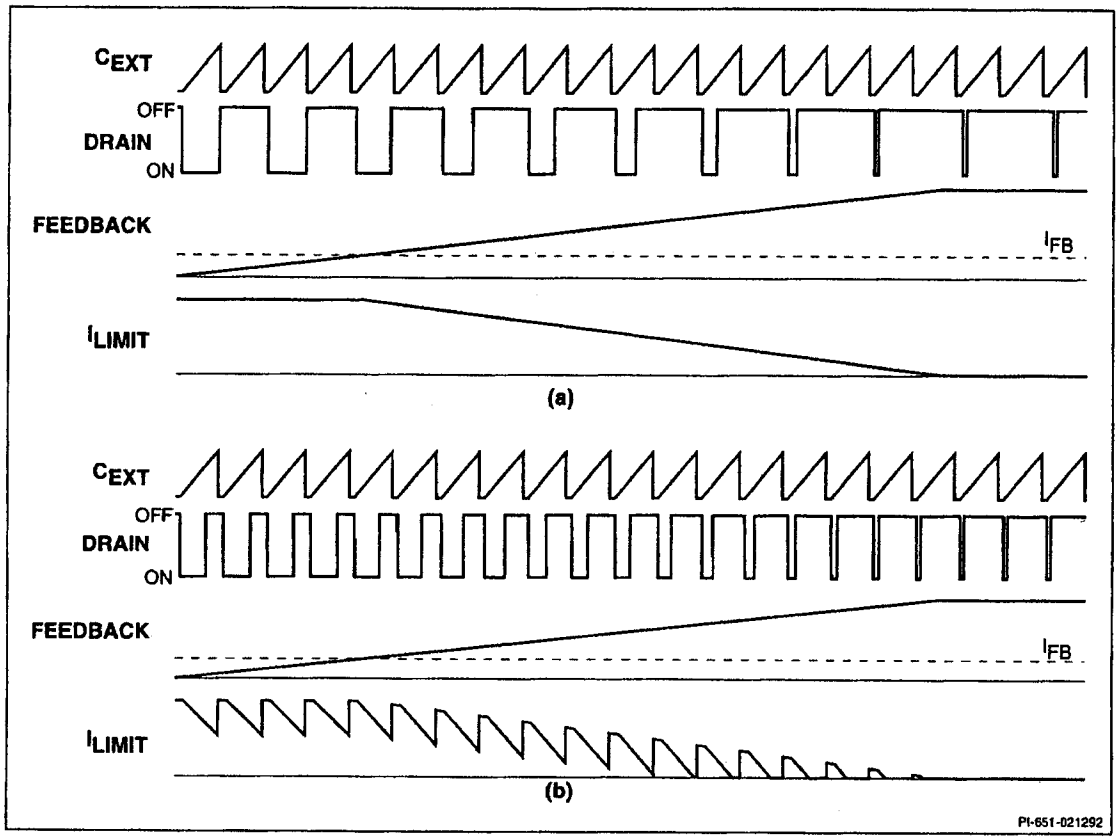

Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode, and (b) 90% Maximum Duty Cycle Mode.

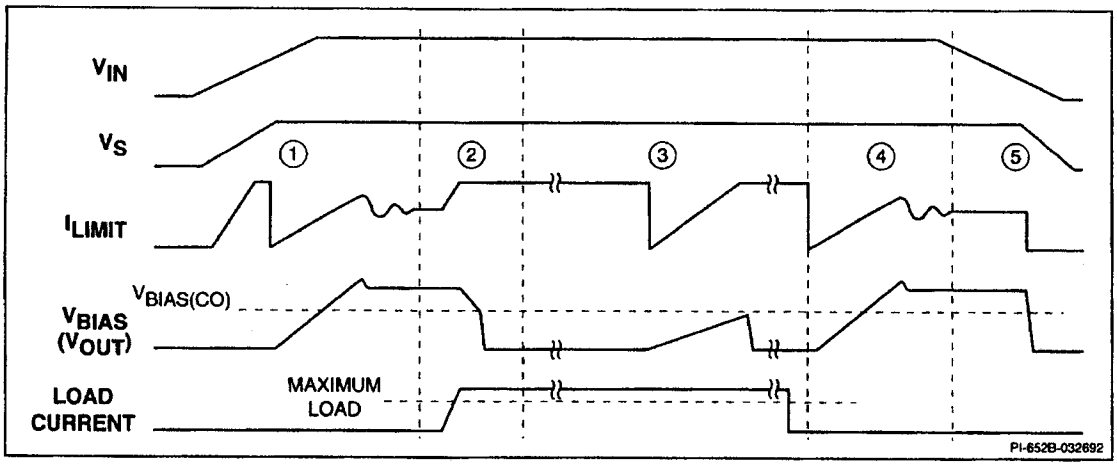

Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

20 W, Universal Off-line Power Supply

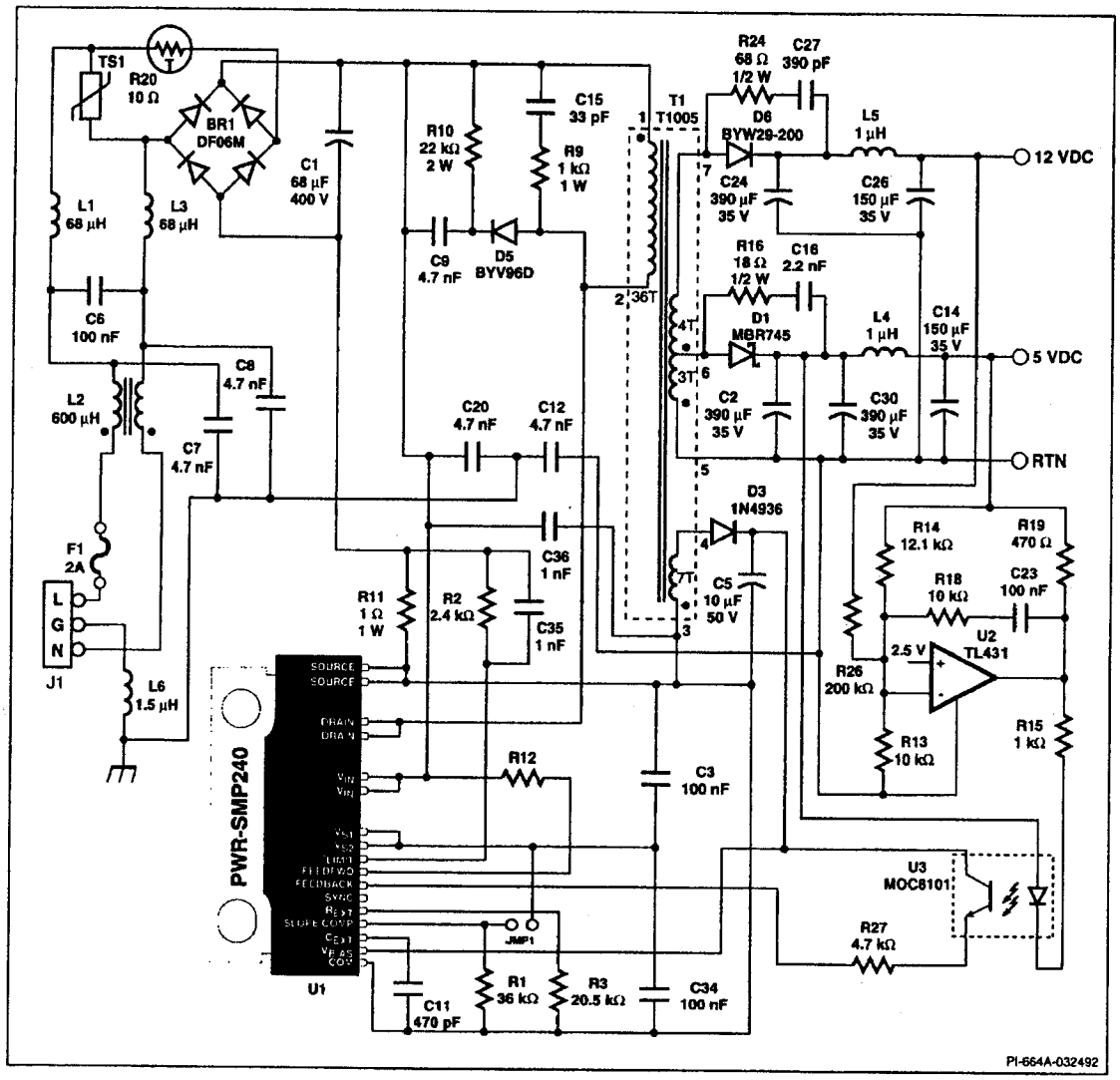

Figure 6. Schematic Diagram of a Single Output 20 W Supply Utilizing the PWR-SMP240.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 20 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SI}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SI}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{BIAS} supply through the optocoupler U3.

The current-mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

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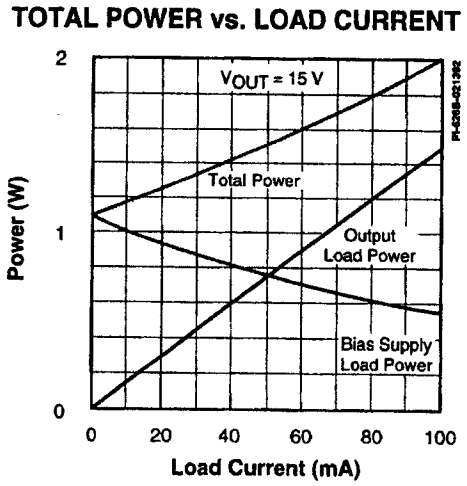


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP240 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{SI} when V_{IN} is between 12 and 20 VDC. The V_{SI} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{SI} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

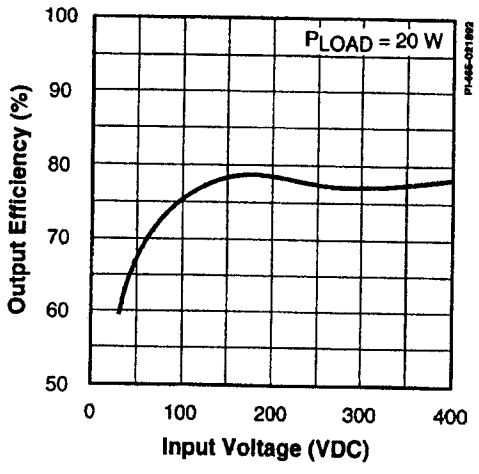
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

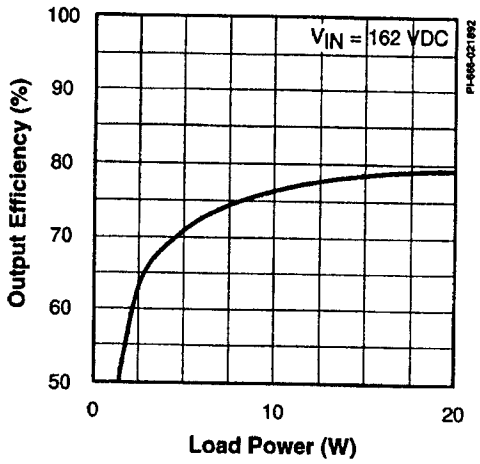
The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL8 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP240. Complete supply specifications are included, as will as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)

EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage ..... 700 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 2 A
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_A = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} =325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(SJ)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{ILIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{ILIMIT}	V_{ILIMIT} = 150 mV		75		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
PULSE WIDTH MODULATOR (cont.)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(ML)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity				±0.5		lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	TYP	MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C			5	Ω
			T_j = 115°C			8.5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		1.2	1.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			200		pF
Output Stored Energy	E_{OSS}				1500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP240 is connected to a high-voltage power source when the test circuit is activated.

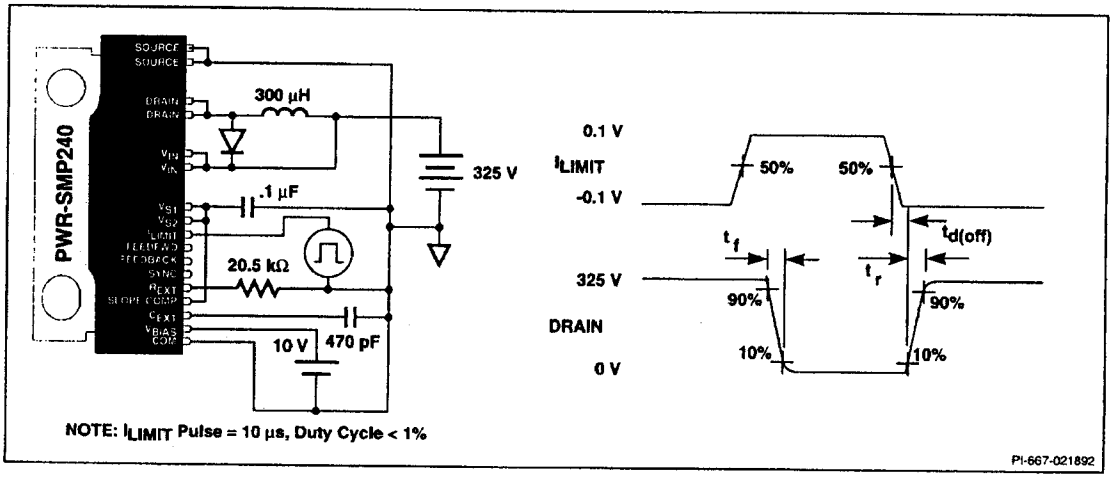
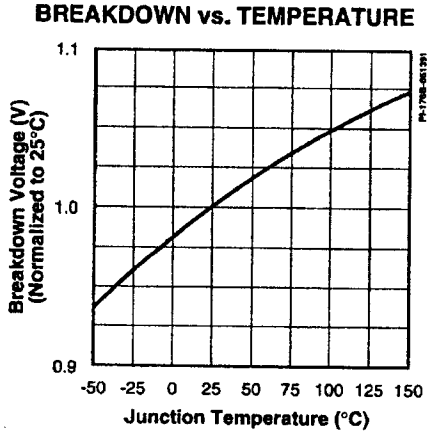
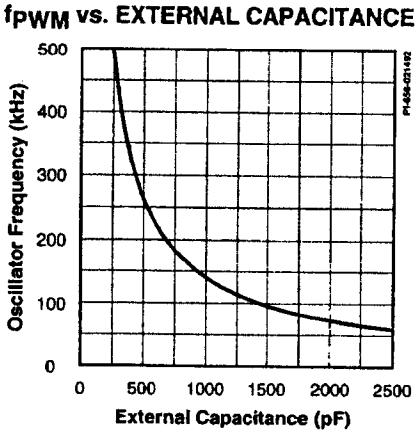


Figure 8. Switching Time Test Circuit.





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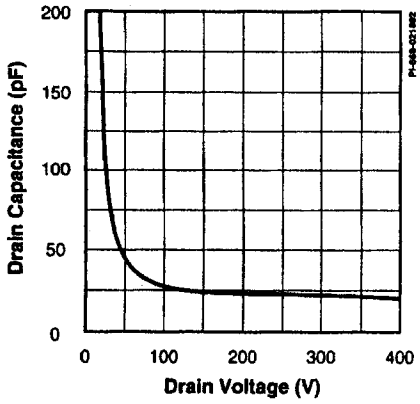
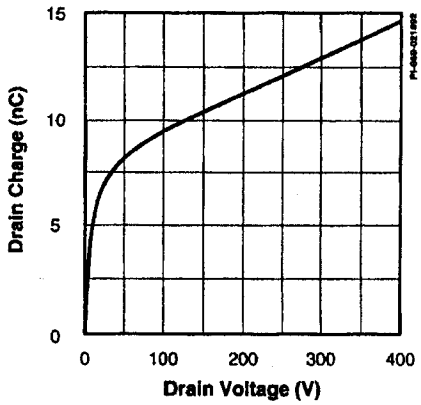
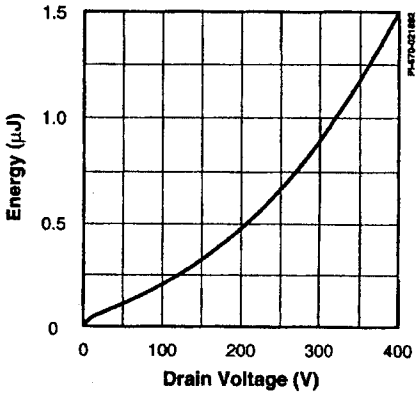
C_{OSS} vs. DRAIN VOLTAGE



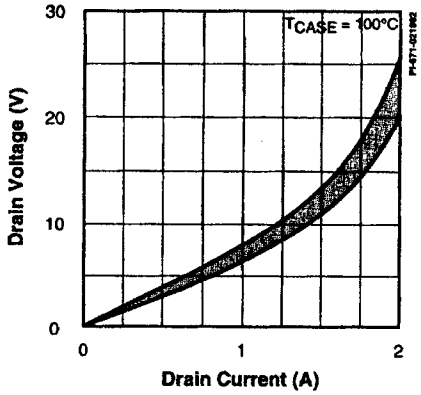
DRAIN CHARGE vs. DRAIN VOLTAGE



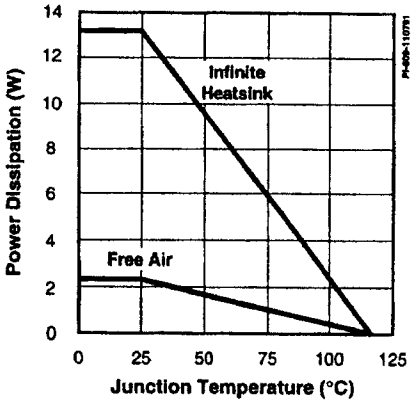
DRAIN CAPACITANCE ENERGY



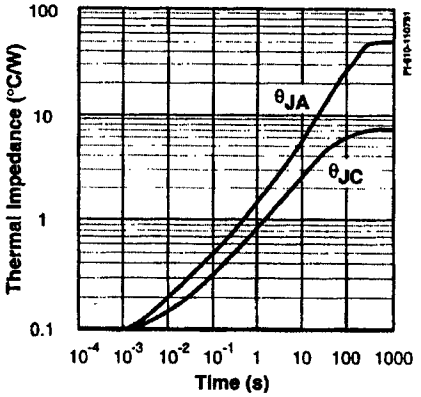
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



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